

FIG. 1

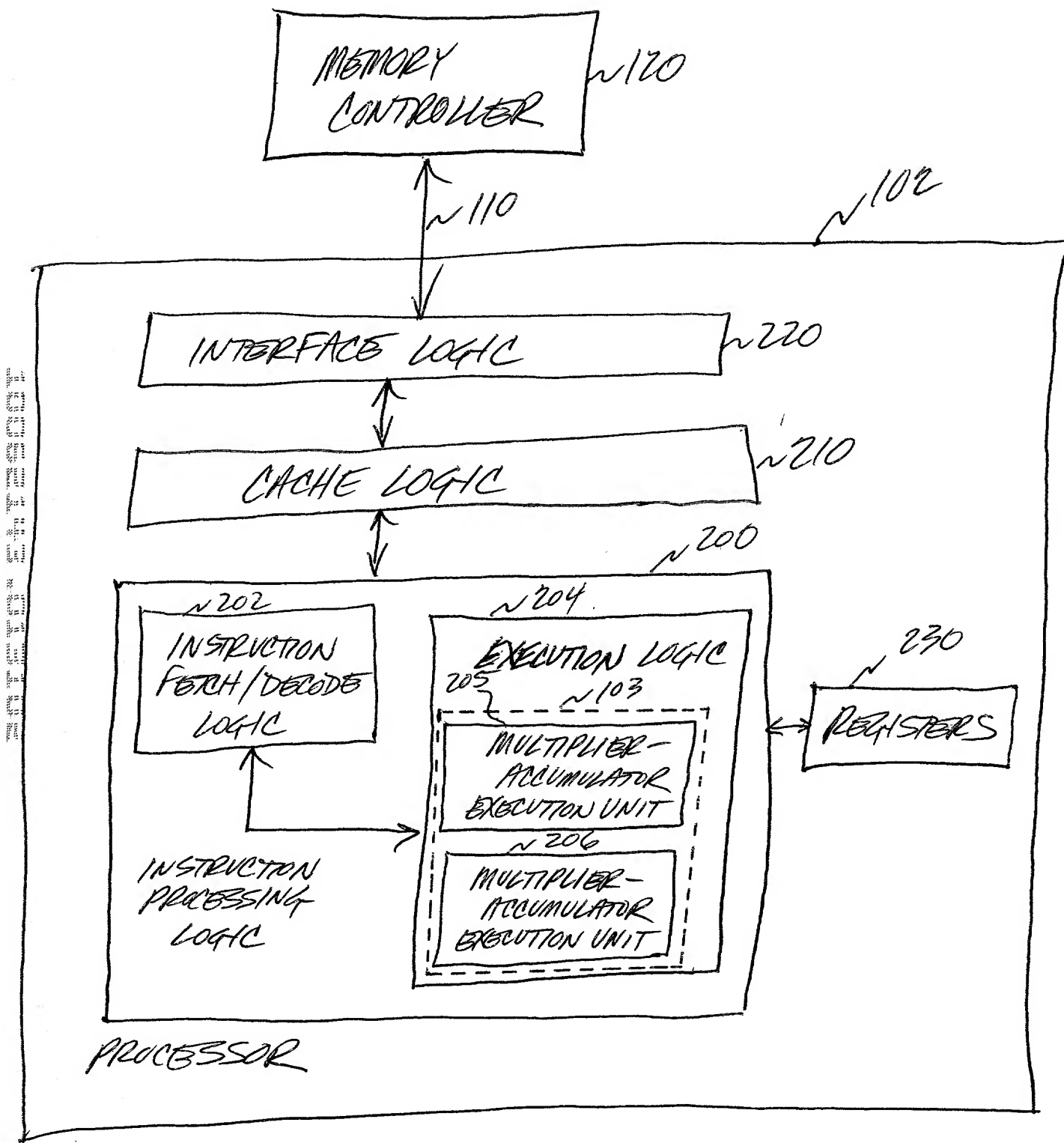


FIG. 2

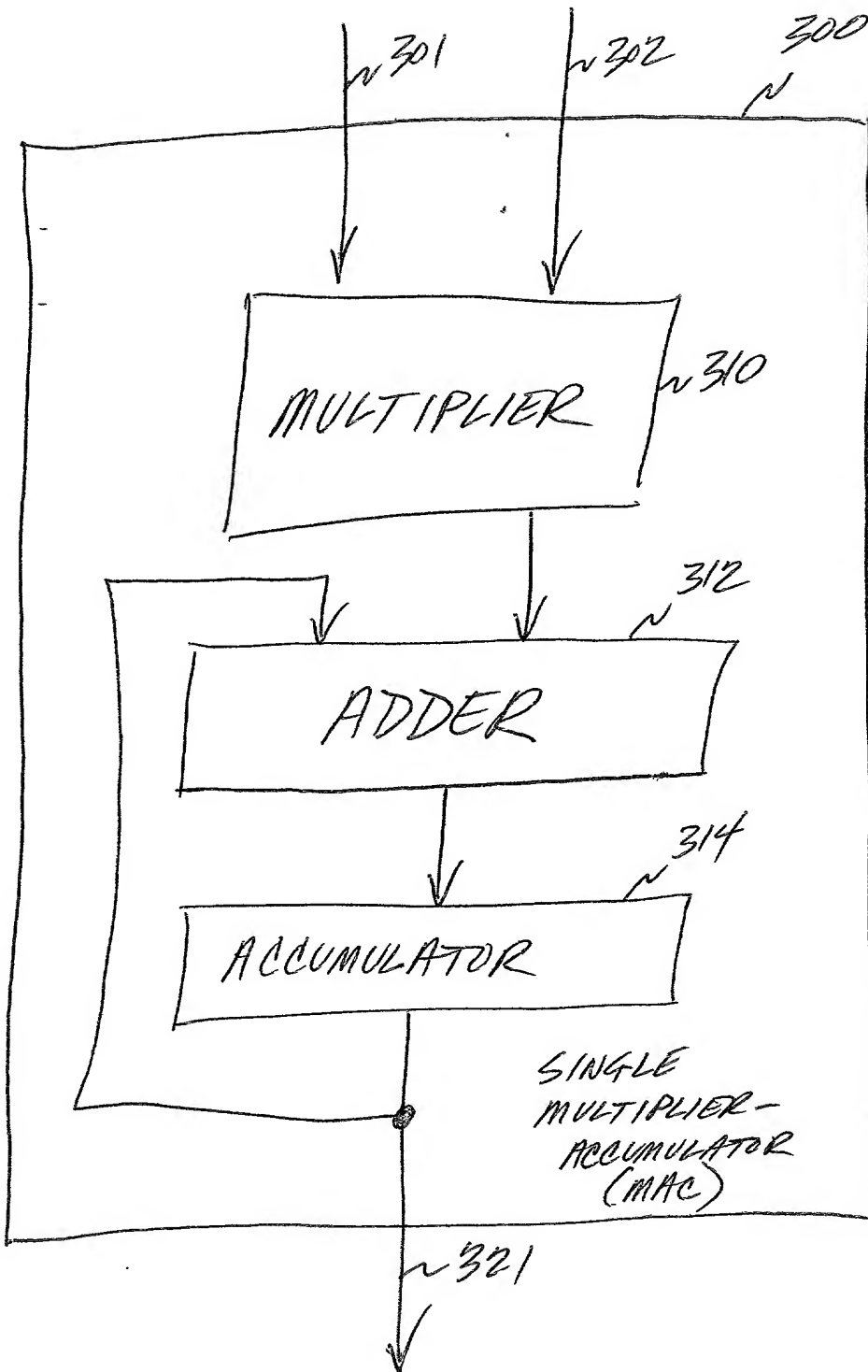


FIG. 3

FIG. 4 is a block diagram of a MAC execution unit block 205. The block 205 includes a control logic 450, a memory/register port(s) 470, a single MAC 411, a single MAC 412, and a buffer 421. The control logic 450 is connected to the single MAC 411 and the single MAC 412. The memory/register port(s) 470 is connected to the single MAC 411 and the buffer 421. The single MAC 411 is connected to the single MAC 412. The buffer 421 is connected to the single MAC 412. The single MAC 411 outputs a signal 431 to the control logic 450. The single MAC 412 outputs a signal 432 to the control logic 450.

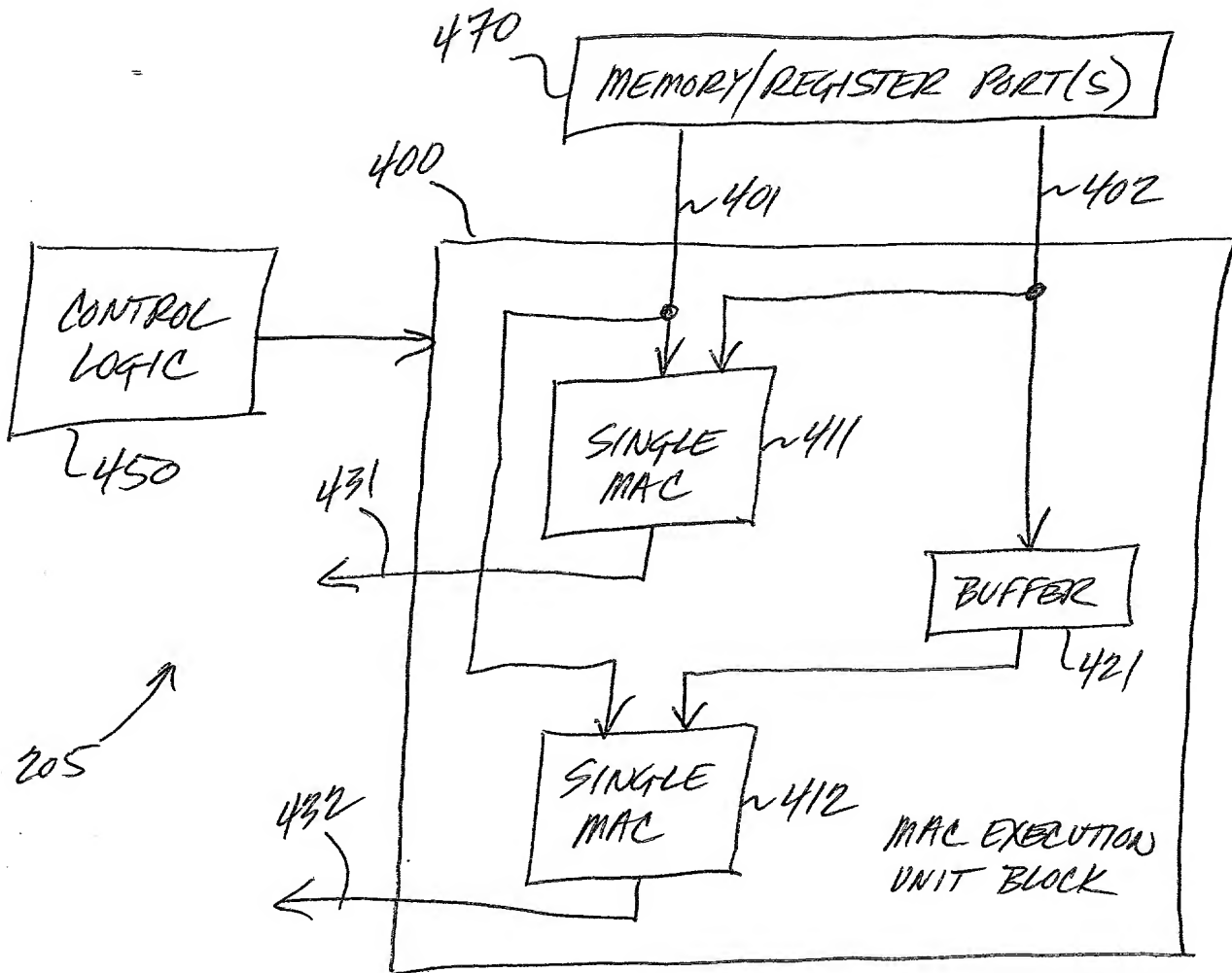


FIG. 4

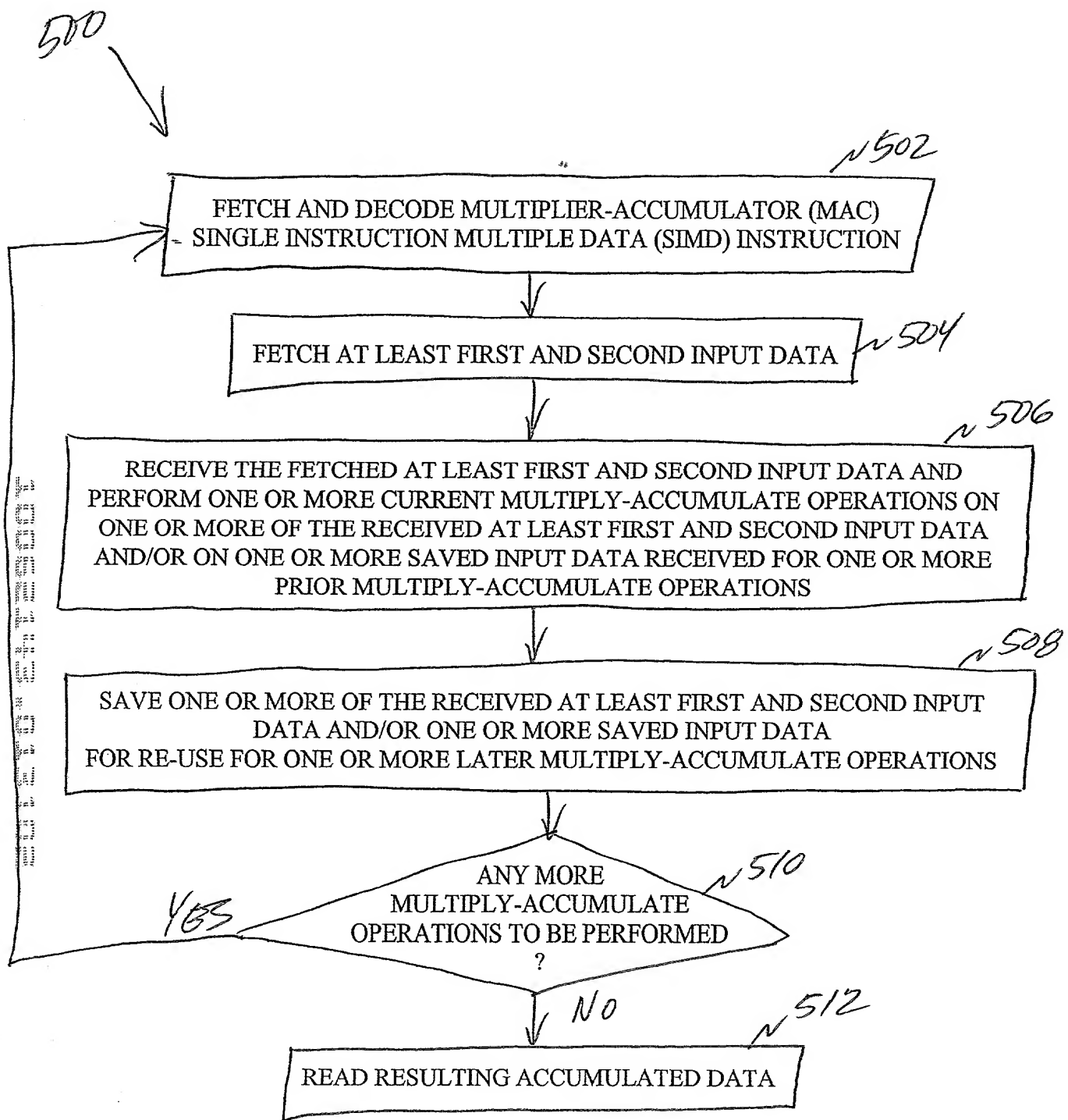


FIG. 5

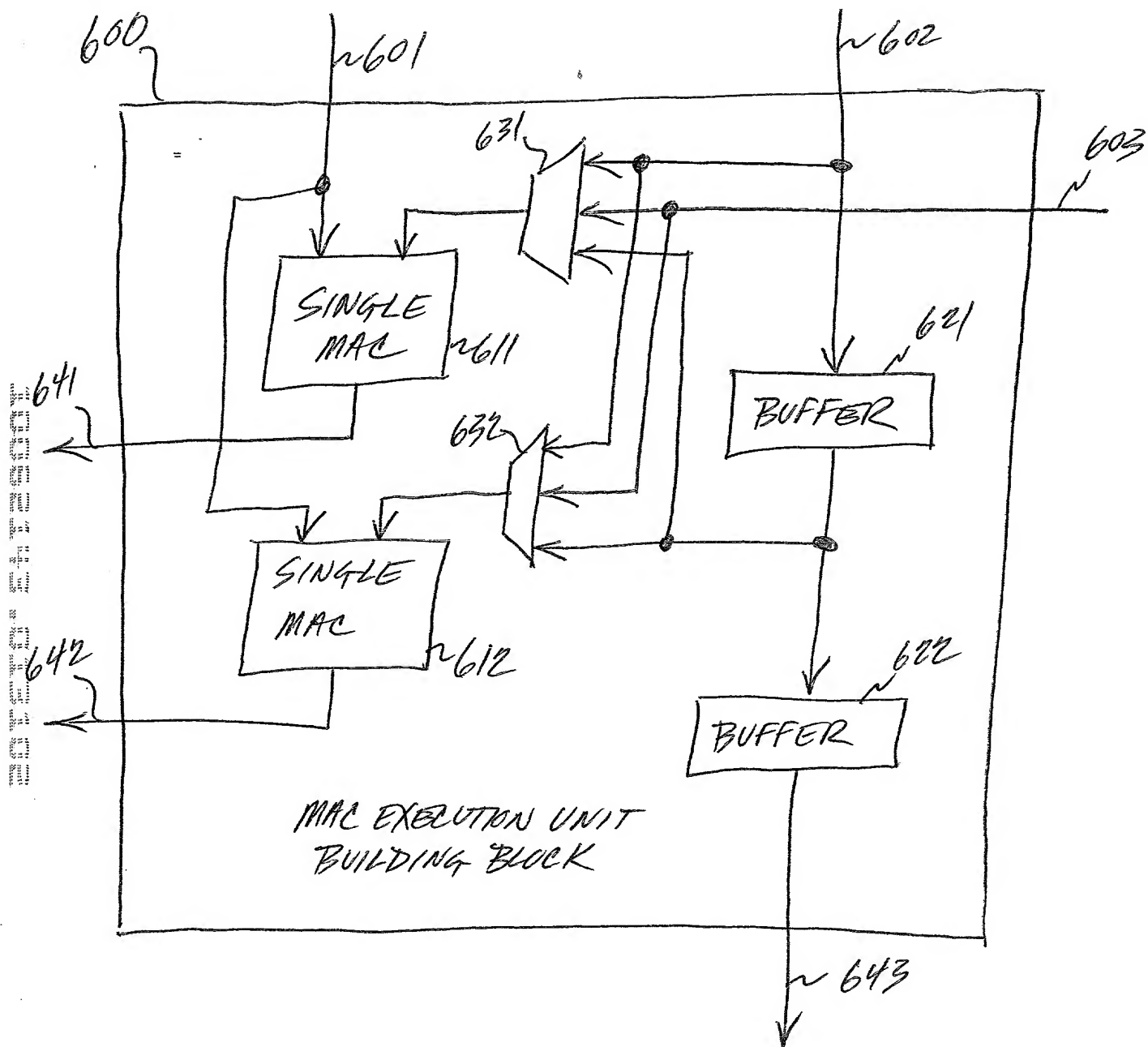


FIG. 6

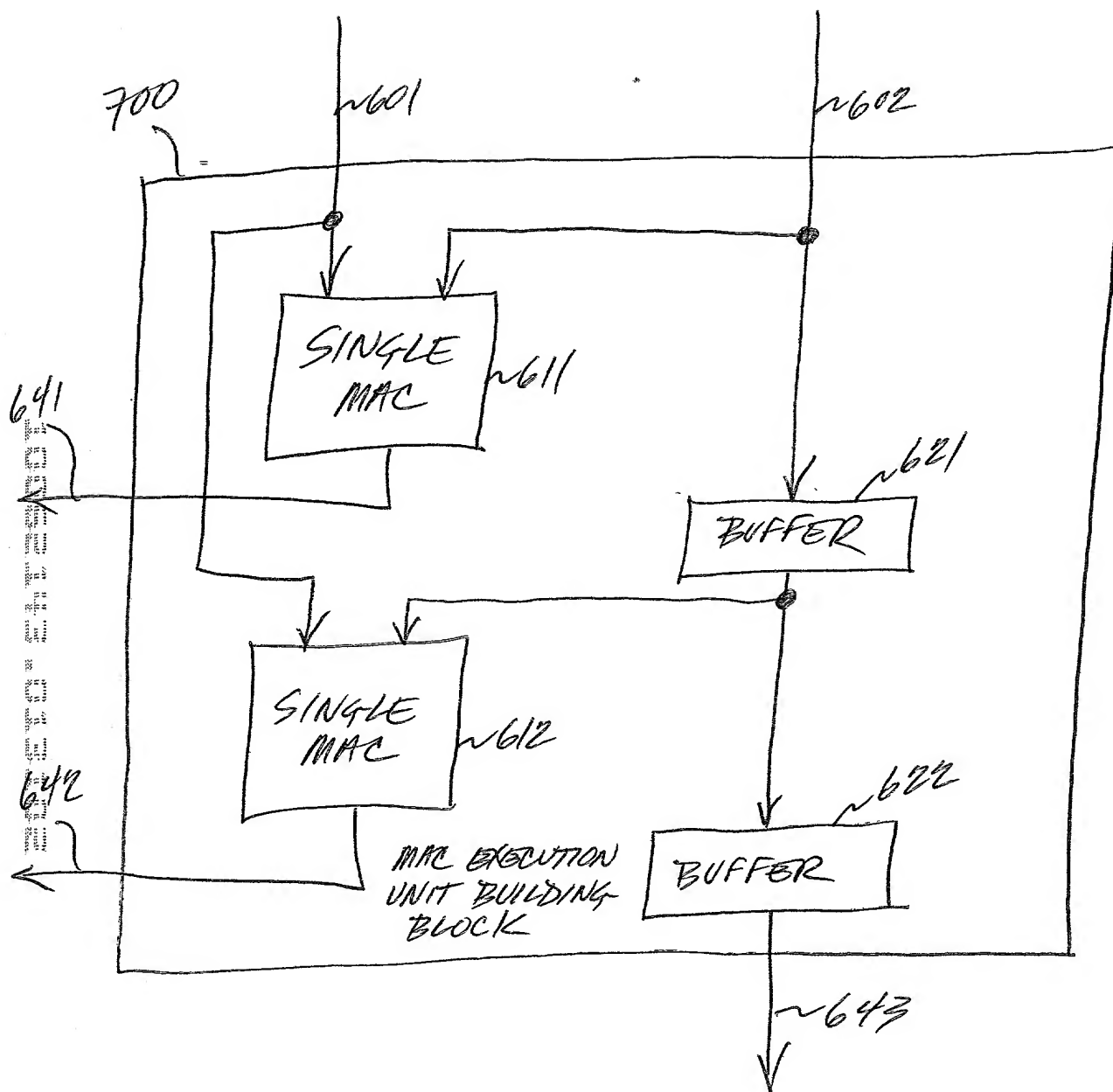


FIG. 7

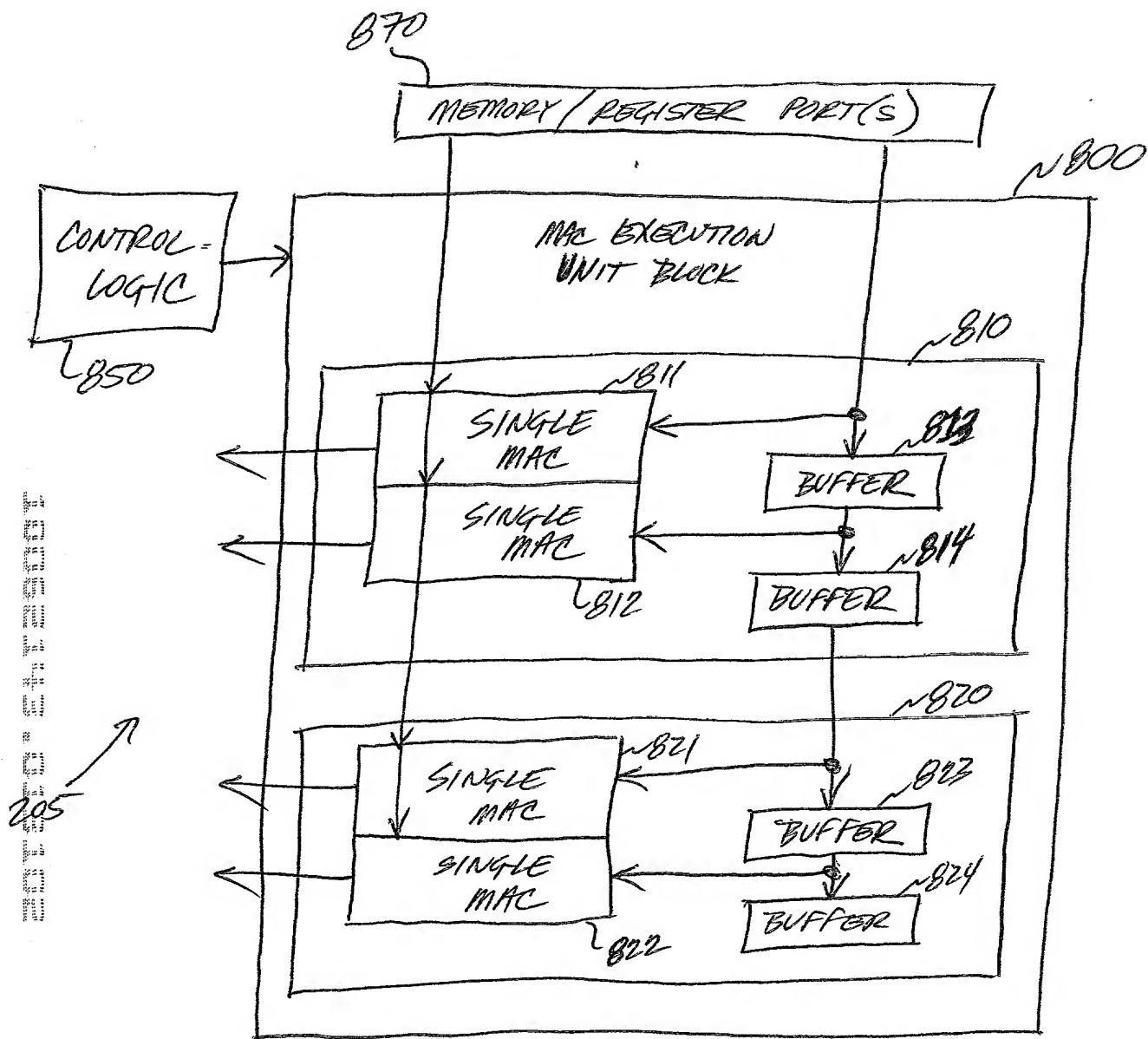


FIG. 8

900
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MAC	Computation Cycle N		Computation Cycle N+1		Computation Cycle N+2	
	1 st MAC Input	2 nd MAC Input	1 st MAC Input	2 nd MAC Input	1 st MAC Input	2 nd MAC Input
811: y(3)	c(31)	x(-28)	c(30)	x(-27)	c(29)	x(-26)
812: y(2)	c(31)	x(-29)	c(30)	x(-28)	c(29)	x(-27)
821: y(1)	c(31)	x(-30)	c(30)	x(-29)	c(29)	x(-28)
822: y(0)	c(31)	x(-31)	c(30)	x(-30)	c(29)	x(-29)

Fig. 9

FIG. 9 is a block diagram of a MAC unit 800. The MAC unit 800 includes a first MAC input 811, a second MAC input 812, a third MAC input 821, and a fourth MAC input 822. The first MAC input 811 is connected to a first MAC input register 811R, which is connected to a first MAC input register output 811RO. The second MAC input 812 is connected to a second MAC input register 812R, which is connected to a second MAC input register output 812RO. The third MAC input 821 is connected to a third MAC input register 821R, which is connected to a third MAC input register output 821RO. The fourth MAC input 822 is connected to a fourth MAC input register 822R, which is connected to a fourth MAC input register output 822RO. The first MAC input register output 811RO is connected to a first MAC input register output register 811RO, which is connected to a first MAC input register output register output 811ROO. The second MAC input register output 812RO is connected to a second MAC input register output register 812RO, which is connected to a second MAC input register output register output 812ROO. The third MAC input register output 821RO is connected to a third MAC input register output register 821RO, which is connected to a third MAC input register output register output 821ROO. The fourth MAC input register output 822RO is connected to a fourth MAC input register output register 822RO, which is connected to a fourth MAC input register output register output 822ROO. The first MAC input register output register output 811ROO is connected to a first MAC input register output register output register output 811ROOO. The second MAC input register output register output 812ROO is connected to a second MAC input register output register output register output 812ROOO. The third MAC input register output register output 821ROO is connected to a third MAC input register output register output register output 821ROOO. The fourth MAC input register output register output 822ROO is connected to a fourth MAC input register output register output register output 822ROOO.

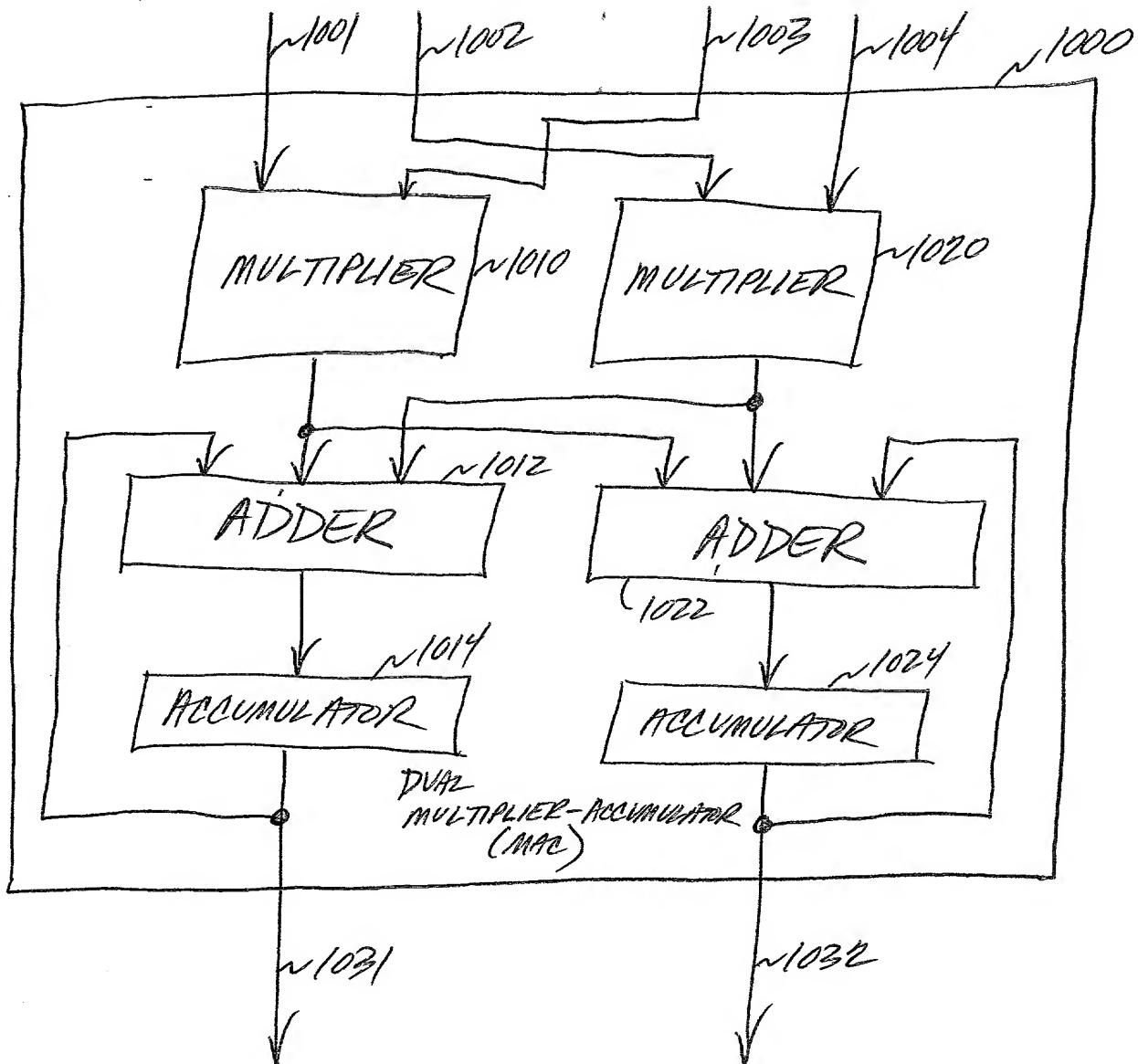


FIG. 10

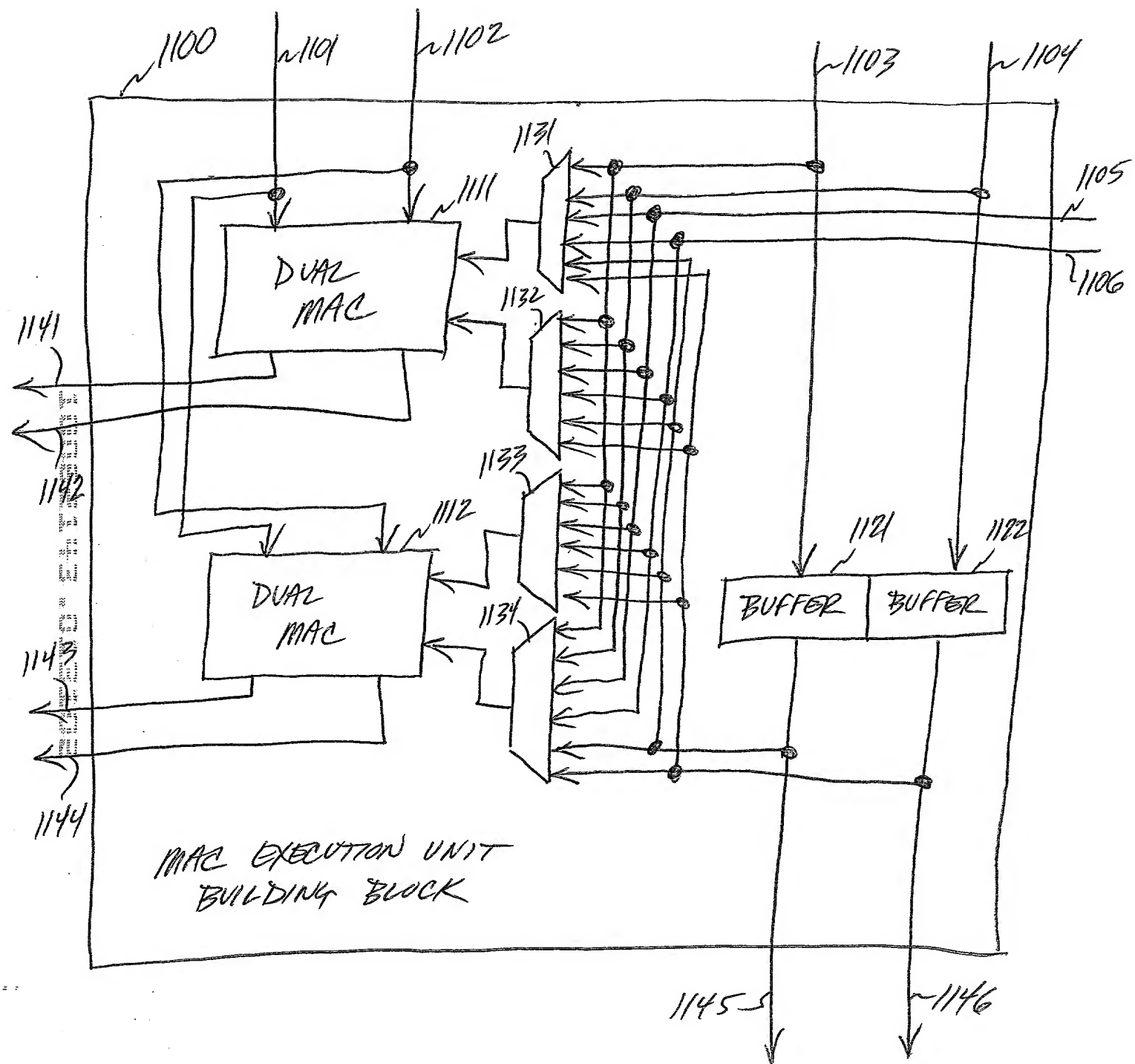


FIG. 11

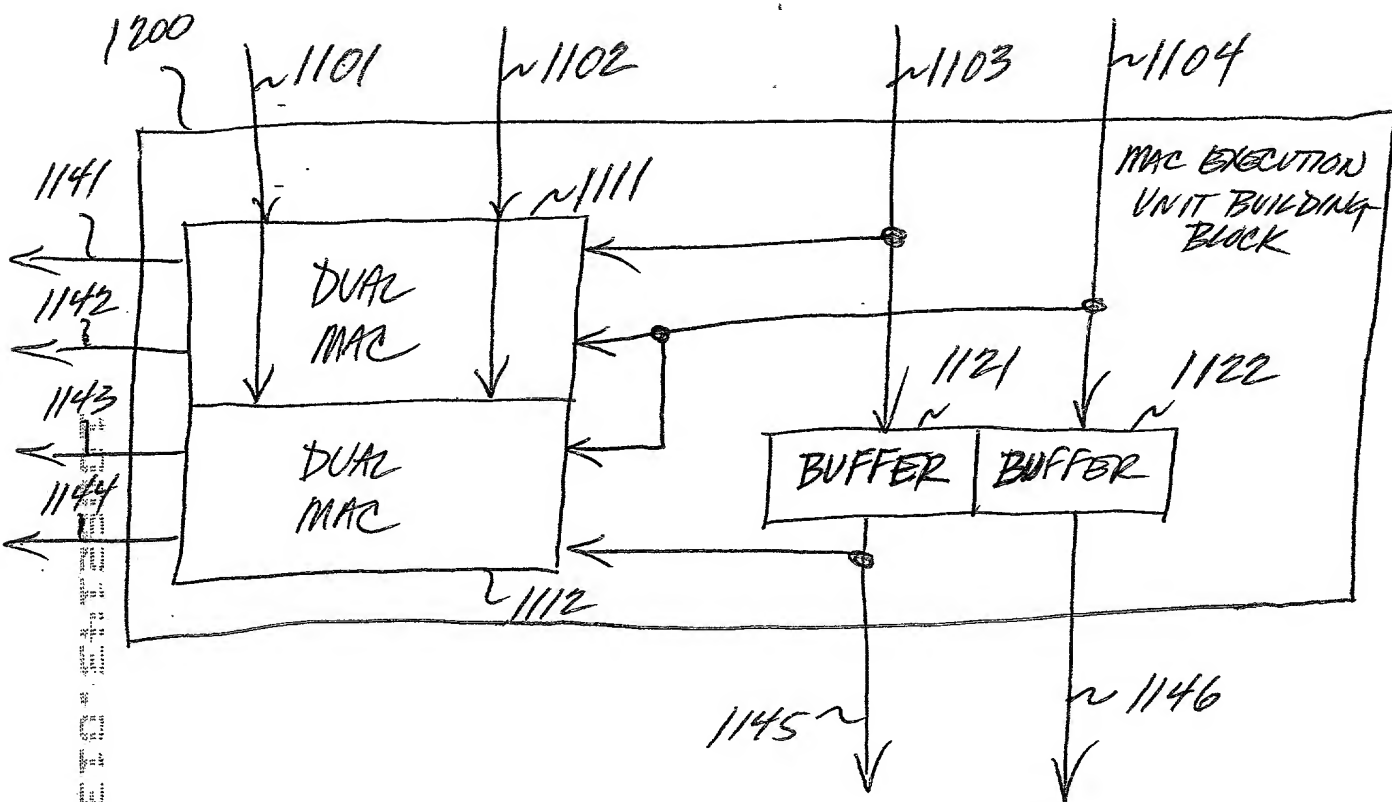


FIG. 12

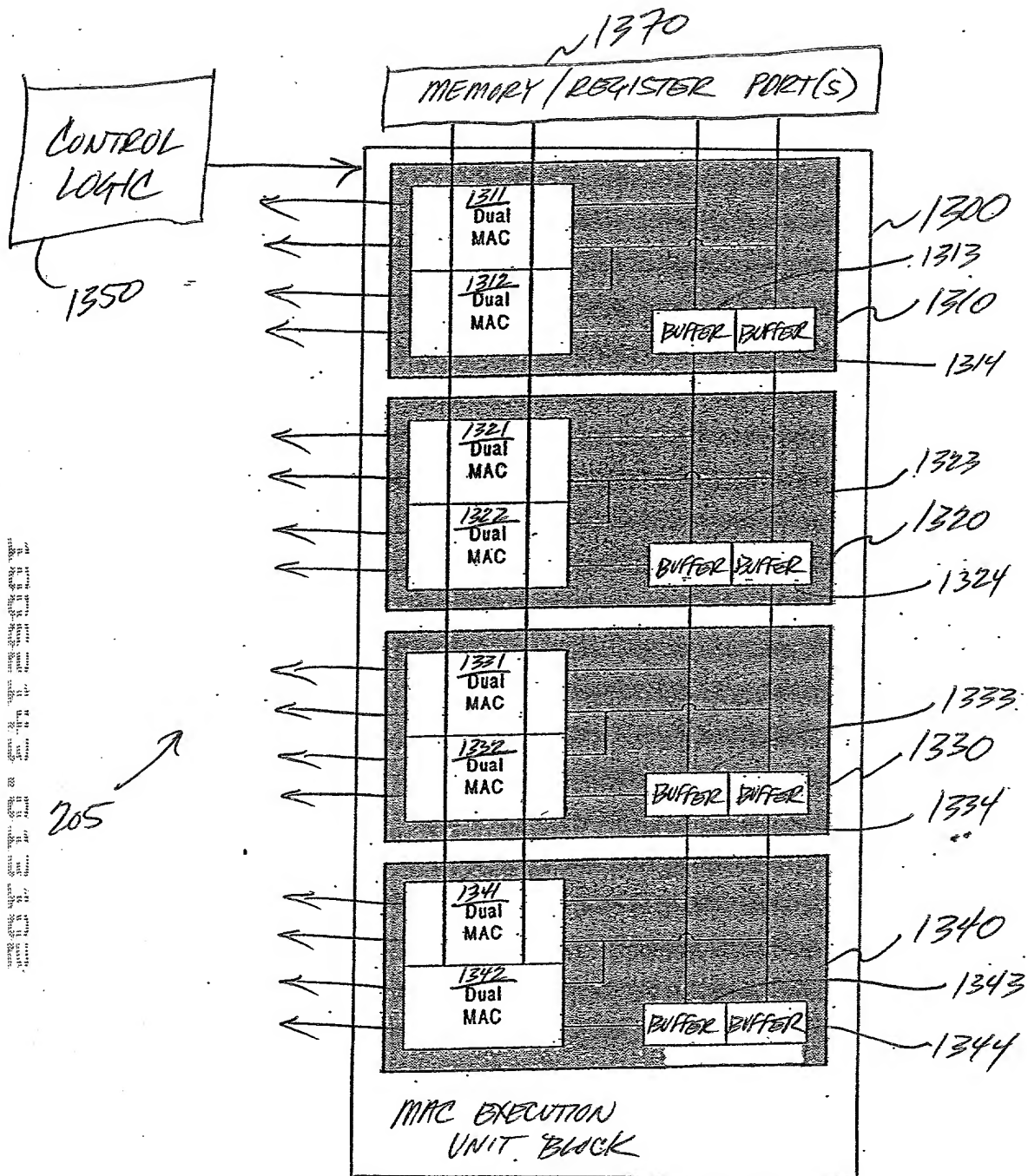


FIG. 13

1400

MAC	Computation Cycle N				Computation Cycle N+1				Computation Cycle N+2			
	1 st MAC Input	3 rd MAC Input	2 nd MAC Input	4 th MAC Input	1 st MAC Input	3 rd MAC Input	2 nd MAC Input	4 th MAC Input	1 st MAC Input	3 rd MAC Input	2 nd MAC Input	4 th MAC Input
1311: y(7)	c(30)	x(-23)	c(31)	x(-24)	c(28)	x(-21)	c(29)	x(-22)	c(26)	x(-19)	c(27)	x(-20)
1312: y(6)	c(30)	x(-24)	c(31)	x(-25)	c(28)	x(-22)	c(29)	x(-23)	c(26)	x(-20)	c(27)	x(-21)
1321: y(5)	c(30)	x(-25)	c(31)	x(-26)	c(28)	x(-23)	c(29)	x(-24)	c(26)	x(-21)	c(27)	x(-22)
1322: y(4)	c(30)	x(-26)	c(31)	x(-27)	c(28)	x(-24)	c(29)	x(-25)	c(26)	x(-22)	c(27)	x(-23)
1331: y(3)	c(30)	x(-27)	c(31)	x(-28)	c(28)	x(-25)	c(29)	x(-26)	c(26)	x(-23)	c(27)	x(-24)
1332: y(2)	c(30)	x(-28)	c(31)	x(-29)	c(28)	x(-26)	c(29)	x(-27)	c(26)	x(-24)	c(27)	x(-25)
1341: y(1)	c(30)	x(-29)	c(31)	x(-30)	c(28)	x(-27)	c(29)	x(-28)	c(26)	x(-25)	c(27)	x(-26)
1342: y(0)	c(30)	x(-30)	c(31)	x(-31)	c(28)	x(-28)	c(29)	x(-29)	c(26)	x(-26)	c(27)	x(-27)

Fig. 14

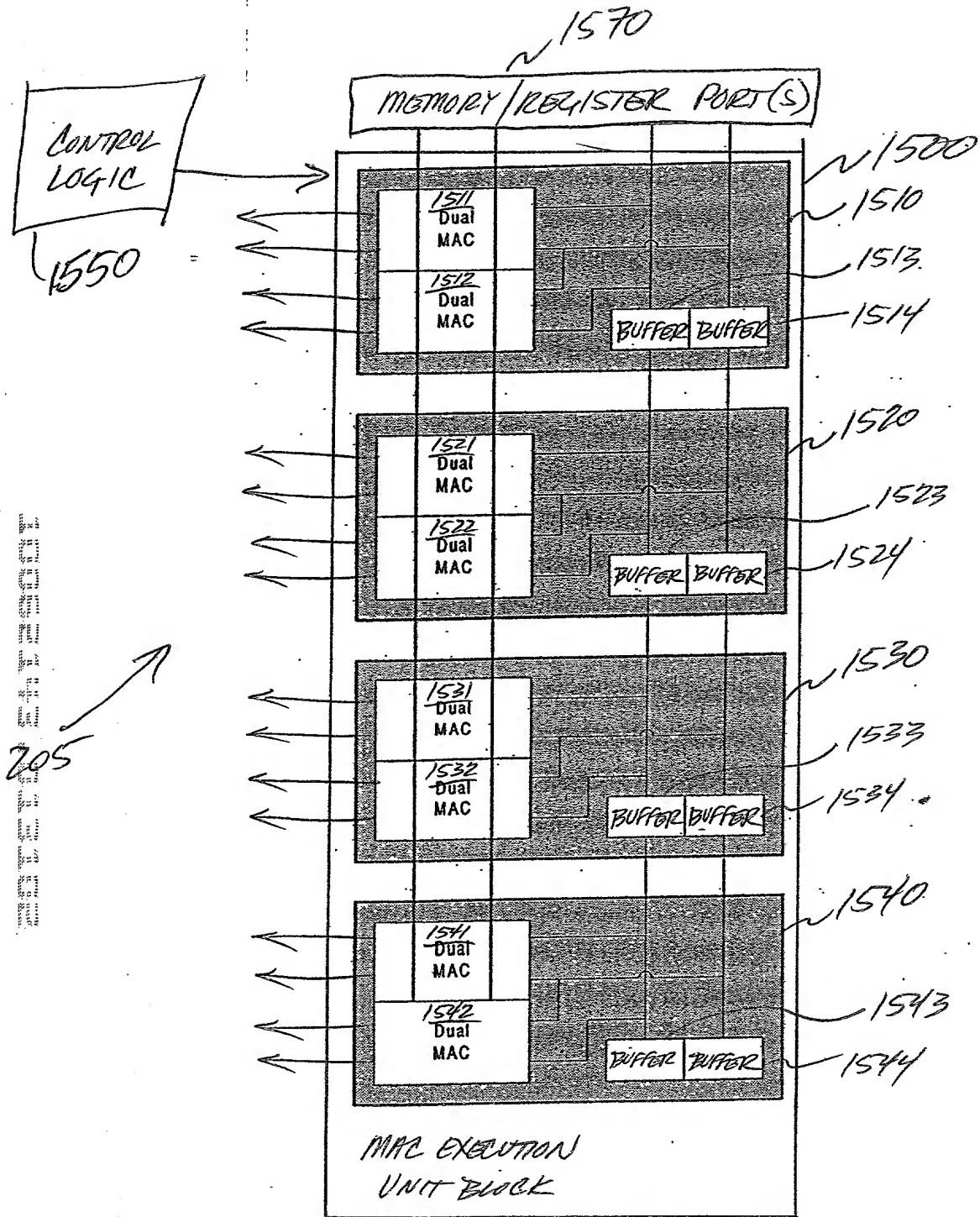


FIG. 15

1600

MAC	Computation Cycle N				Computation Cycle N+1				Computation Cycle N+2			
	1 st MAC Input	3 rd MAC Input	2 nd MAC Input	4 th MAC Input	1 st MAC Input	3 rd MAC Input	2 nd MAC Input	4 th MAC Input	1 st MAC Input	3 rd MAC Input	2 nd MAC Input	4 th MAC Input
1511: y(3) _r	c(31) _r	x(-28) _r	c(31) _i	x(-28) _i	c(30) _r	x(-27) _r	c(30) _i	x(-27) _i	c(29) _r	x(-26) _r	c(29) _i	x(-26) _i
1512: y(3) _i	c(31) _r	x(-28) _i	c(31) _i	x(-28) _r	c(30) _r	x(-27) _i	c(30) _i	x(-27) _r	c(29) _r	x(-26) _i	c(29) _i	x(-26) _r
1521: y(2) _r	c(31) _r	x(-29) _r	c(31) _i	x(-29) _i	c(30) _r	x(-28) _r	c(30) _i	x(-28) _i	c(29) _r	x(-27) _r	c(29) _i	x(-27) _i
1522: y(2) _i	c(31) _r	x(-29) _i	c(31) _i	x(-29) _r	c(30) _r	x(-28) _i	c(30) _i	x(-28) _r	c(29) _r	x(-27) _i	c(29) _i	x(-27) _r
1531: y(1) _r	c(31) _r	x(-30) _r	c(31) _i	x(-30) _i	c(30) _r	x(-29) _r	c(30) _i	x(-29) _i	c(29) _r	x(-28) _r	c(29) _i	x(-28) _i
1532: y(1) _i	c(31) _r	x(-30) _i	c(31) _i	x(-30) _r	c(30) _r	x(-29) _i	c(30) _i	x(-29) _r	c(29) _r	x(-28) _i	c(29) _i	x(-28) _r
1541: y(0) _r	c(31) _r	x(-31) _r	c(31) _i	x(-31) _i	c(30) _r	x(-30) _r	c(30) _i	x(-30) _i	c(29) _r	x(-29) _r	c(29) _i	x(-29) _i
1542: y(0) _i	c(31) _r	x(-31) _i	c(31) _i	x(-31) _r	c(30) _r	x(-30) _i	c(30) _i	x(-30) _r	c(29) _r	x(-29) _i	c(29) _i	x(-29) _r

Fig. 16

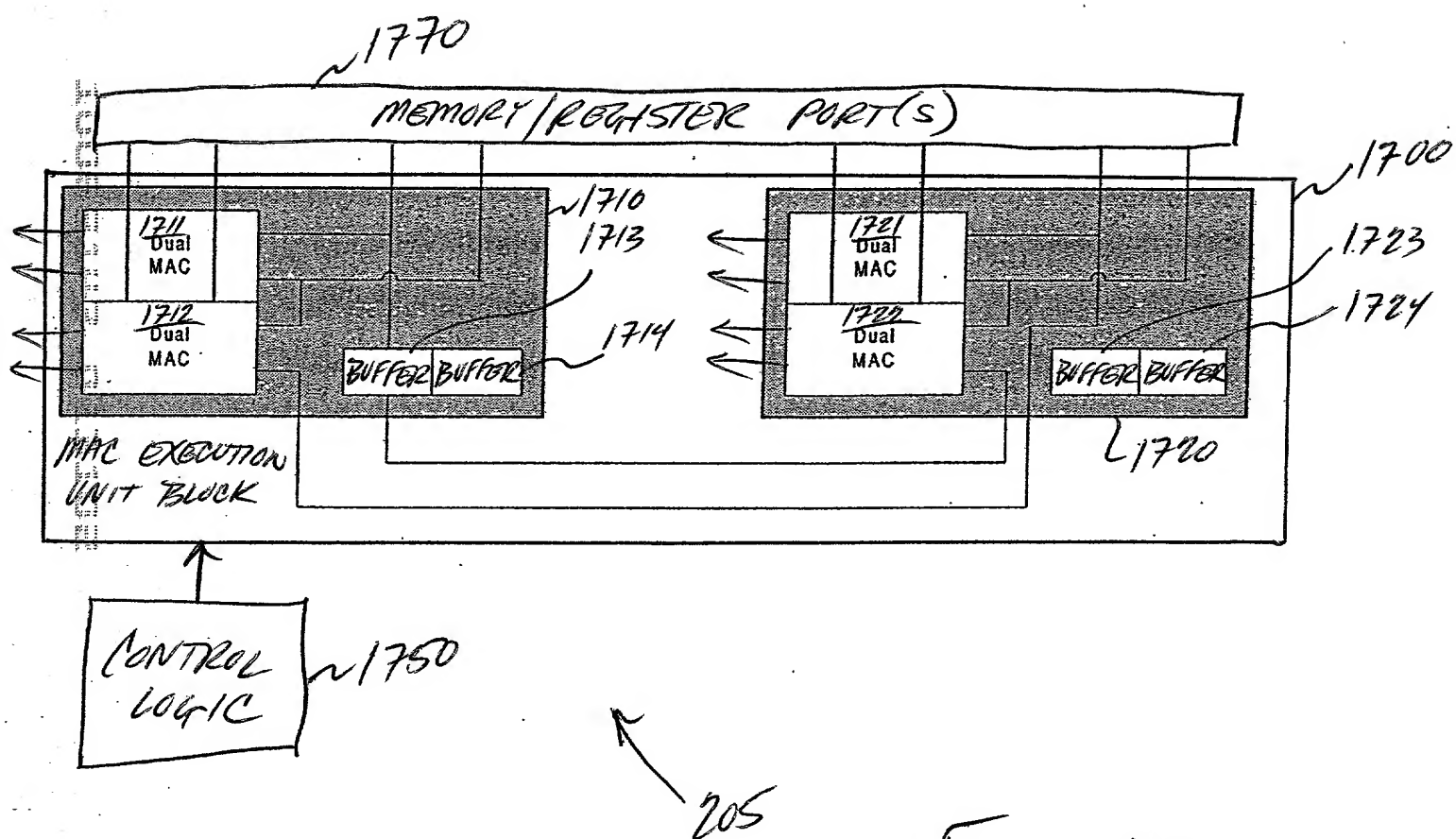


FIG. 17

1800
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Computation Cycle N									
MAC	1 st MAC Input	3 rd MAC Input	2 nd MAC Input	4 th MAC Input	MAC	1 st MAC Input	3 rd MAC Input	2 nd MAC Input	4 th MAC Input
1711: y(1)	c(28)	x(-27)	c(29)	x(-28)	1721: y(1)	c(30)	x(-29)	c(31)	x(-30)
1712: y(0)	c(28)	x(-28)	c(29)	x(-29)	1722: y(0)	c(30)	x(-30)	c(31)	x(-31)
Computation Cycle N+1									
MAC	1 st MAC Input	3 rd MAC Input	2 nd MAC Input	4 th MAC Input	MAC	1 st MAC Input	3 rd MAC Input	2 nd MAC Input	4 th MAC Input
1711: y(1)	c(24)	x(-23)	c(25)	x(-24)	1721: y(1)	c(26)	x(-25)	c(27)	x(-26)
1712: y(0)	c(24)	x(-24)	c(25)	x(-25)	1722: y(0)	c(26)	x(-26)	c(27)	x(-27)
Computation Cycle N+2									
MAC	1 st MAC Input	3 rd MAC Input	2 nd MAC Input	4 th MAC Input	MAC	1 st MAC Input	3 rd MAC Input	2 nd MAC Input	4 th MAC Input
1711: y(1)	c(20)	x(-19)	c(21)	x(-20)	1721: y(1)	c(22)	x(-21)	c(23)	x(-22)
1712: y(0)	c(20)	x(-20)	c(21)	x(-21)	1722: y(0)	c(22)	x(-22)	c(23)	x(-23)

Fig. 18

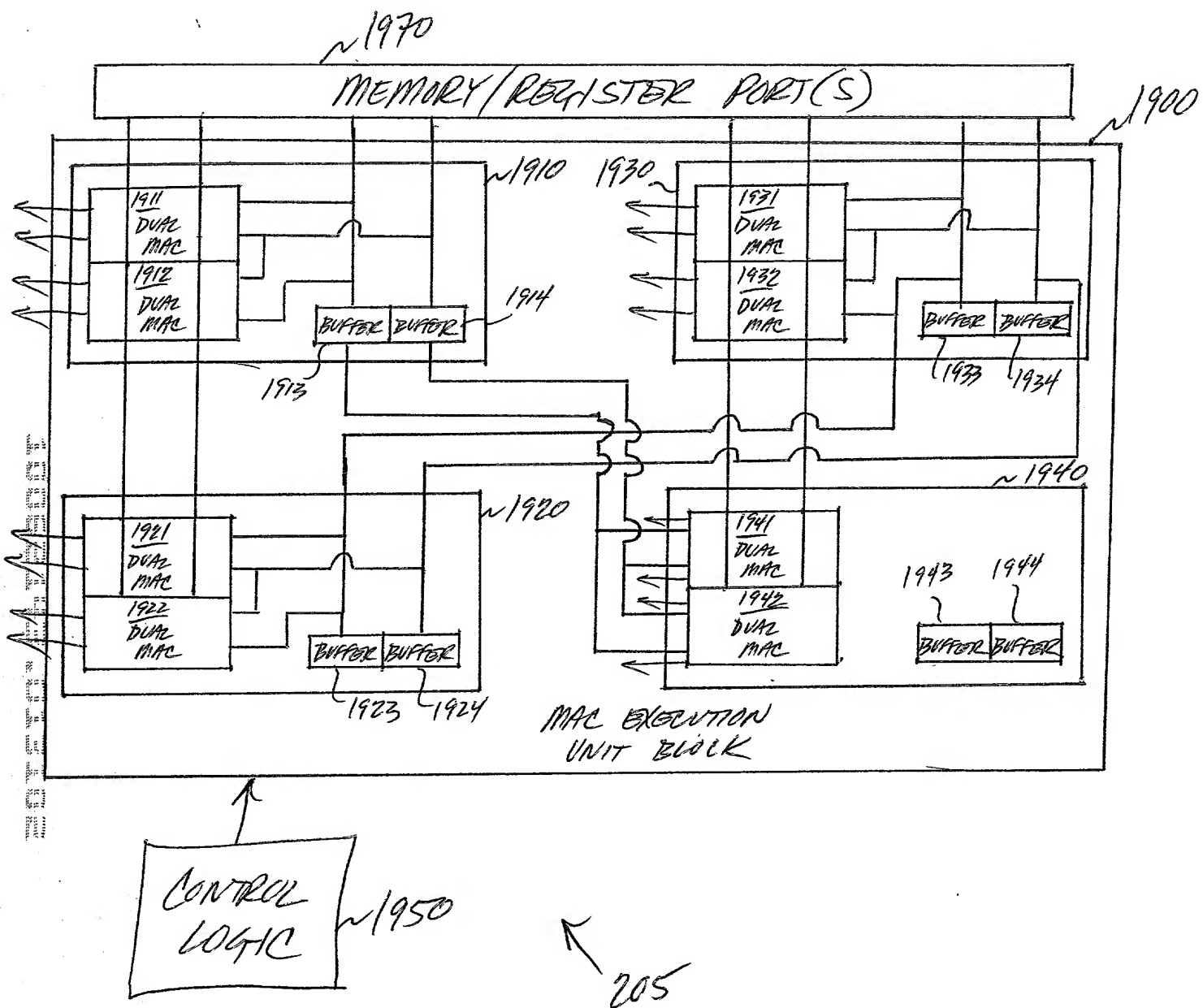


FIG. 19

2090
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Computation Cycle N									
MAC	1 st MAC Input	3 rd MAC Input	2 nd MAC Input	4 th MAC Input	MAC	1 st MAC Input	3 rd MAC Input	2 nd MAC Input	4 th MAC Input
1911: $y(1)_r$	$c(30)_r$	$x(-29)_r$	$c(30)_i$	$x(-29)_i$	1931: $y(1)_r$	$c(31)_r$	$x(-30)_r$	$c(31)_i$	$x(-30)_i$
1912: $y(1)_i$	$c(30)_r$	$x(-29)_i$	$c(30)_i$	$x(-29)_r$	1932: $y(1)_i$	$c(31)_r$	$x(-30)_i$	$c(31)_i$	$x(-30)_r$
1921: $y(0)_r$	$c(30)_r$	$x(-30)_r$	$c(30)_i$	$x(-30)_i$	1941: $y(0)_r$	$c(31)_r$	$x(-31)_r$	$c(31)_i$	$x(-31)_i$
1922: $y(0)_i$	$c(30)_r$	$x(-30)_i$	$c(30)_i$	$x(-30)_r$	1942: $y(0)_i$	$c(31)_r$	$x(-31)_i$	$c(31)_i$	$x(-31)_r$
Computation Cycle N+1									
MAC	1 st MAC Input	3 rd MAC Input	2 nd MAC Input	4 th MAC Input	MAC	1 st MAC Input	3 rd MAC Input	2 nd MAC Input	4 th MAC Input
1911: $y(1)_r$	$c(28)_r$	$x(-27)_r$	$c(28)_i$	$x(-27)_i$	1931: $y(1)_r$	$c(29)_r$	$x(-28)_r$	$c(29)_i$	$x(-28)_i$
1912: $y(1)_i$	$c(28)_r$	$x(-27)_i$	$c(28)_i$	$x(-27)_r$	1932: $y(1)_i$	$c(29)_r$	$x(-28)_i$	$c(29)_i$	$x(-28)_r$
1921: $y(0)_r$	$c(28)_r$	$x(-28)_r$	$c(28)_i$	$x(-28)_i$	1941: $y(0)_r$	$c(29)_r$	$x(-29)_r$	$c(29)_i$	$x(-29)_i$
1922: $y(0)_i$	$c(28)_r$	$x(-28)_i$	$c(28)_i$	$x(-28)_r$	1942: $y(0)_i$	$c(29)_r$	$x(-29)_i$	$c(29)_i$	$x(-29)_r$
Computation Cycle N+2									
MAC	1 st MAC Input	3 rd MAC Input	2 nd MAC Input	4 th MAC Input	MAC	1 st MAC Input	3 rd MAC Input	2 nd MAC Input	4 th MAC Input
1911: $y(1)_r$	$c(26)_r$	$x(-25)_r$	$c(26)_i$	$x(-25)_i$	1931: $y(1)_r$	$c(27)_r$	$x(-26)_r$	$c(27)_i$	$x(-26)_i$
1912: $y(1)_i$	$c(26)_r$	$x(-25)_i$	$c(26)_i$	$x(-25)_r$	1932: $y(1)_i$	$c(27)_r$	$x(-26)_i$	$c(27)_i$	$x(-26)_r$
1921: $y(0)_r$	$c(26)_r$	$x(-26)_r$	$c(26)_i$	$x(-26)_i$	1941: $y(0)_r$	$c(27)_r$	$x(-27)_r$	$c(27)_i$	$x(-27)_i$
1922: $y(0)_i$	$c(26)_r$	$x(-26)_i$	$c(26)_i$	$x(-26)_r$	1942: $y(0)_i$	$c(27)_r$	$x(-27)_i$	$c(27)_i$	$x(-27)_r$

Fig. 20

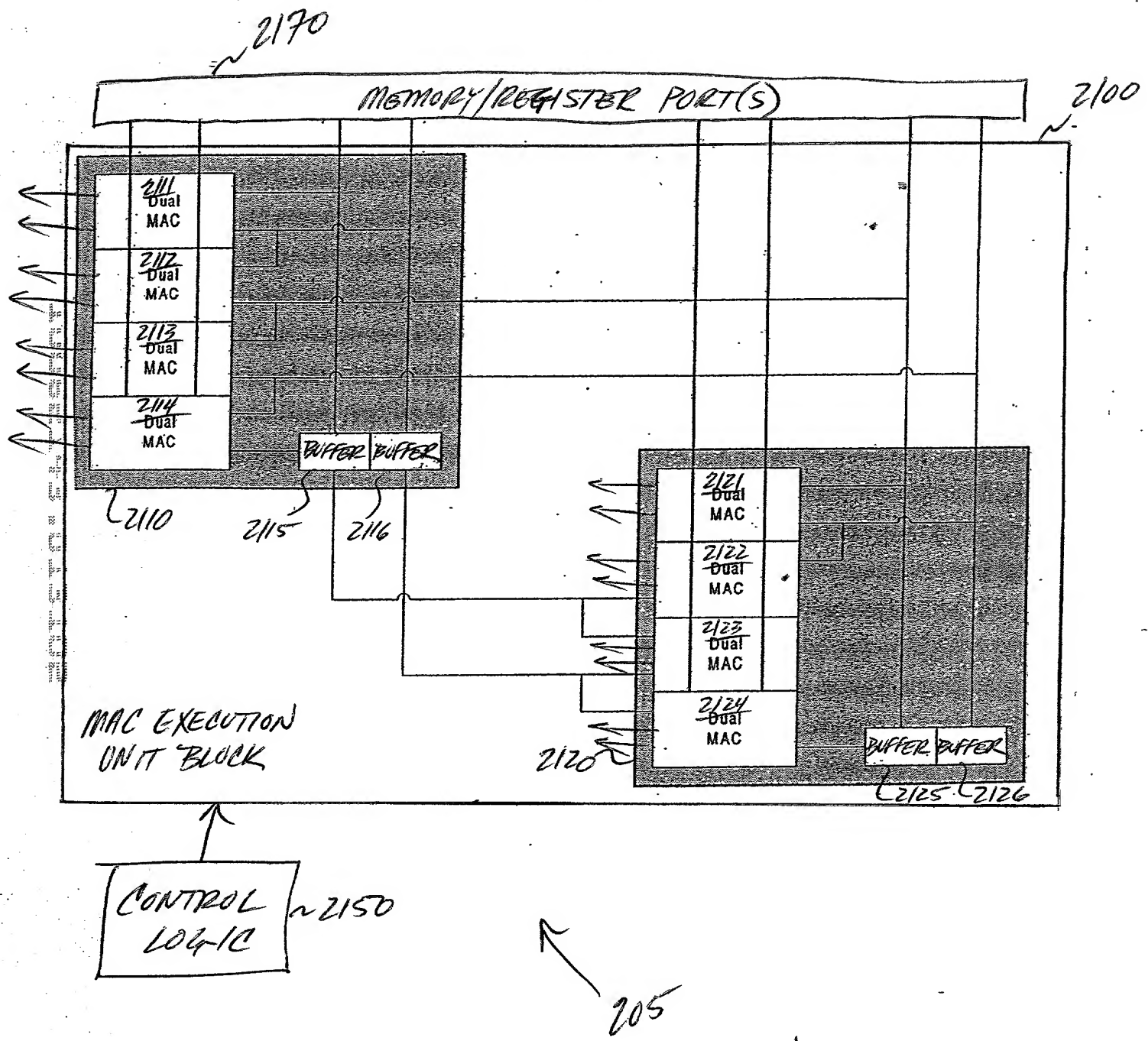


FIG. 21

2200 ↘

Computation Cycle N									
MAC	1 st MAC Input	3 rd MAC Input	2 nd MAC Input	4 th MAC Input	MAC	1 st MAC Input	3 rd MAC Input	2 nd MAC Input	4 th MAC Input
2111: y(3)	c(28)	x(-25)	c(29)	x(-26)	2121: y(3)	c(30)	x(-27)	c(31)	x(-28)
2112: y(2)	c(28)	x(-26)	c(29)	x(-27)	2122: y(2)	c(30)	x(-28)	c(31)	x(-29)
2113: y(1)	c(28)	x(-27)	c(29)	x(-28)	2123: y(1)	c(30)	x(-29)	c(31)	x(-30)
2114: y(0)	c(28)	x(-28)	c(29)	x(-29)	2124: y(0)	c(30)	x(-30)	c(31)	x(-31)
Computation Cycle N+1									
MAC	1 st MAC Input	3 rd MAC Input	2 nd MAC Input	4 th MAC Input	MAC	1 st MAC Input	3 rd MAC Input	2 nd MAC Input	4 th MAC Input
2111: y(3)	c(24)	x(-21)	c(25)	x(-22)	2121: y(3)	c(26)	x(-23)	c(27)	x(-24)
2112: y(2)	c(24)	x(-22)	c(25)	x(-23)	2122: y(2)	c(26)	x(-24)	c(27)	x(-25)
2113: y(1)	c(24)	x(-23)	c(25)	x(-24)	2123: y(1)	c(26)	x(-25)	c(27)	x(-26)
2114: y(0)	c(24)	x(-24)	c(25)	x(-25)	2124: y(0)	c(26)	x(-26)	c(27)	x(-27)
Computation Cycle N+2									
MAC	1 st MAC Input	3 rd MAC Input	2 nd MAC Input	4 th MAC Input	MAC	1 st MAC Input	3 rd MAC Input	2 nd MAC Input	4 th MAC Input
2111: y(3)	c(20)	x(-17)	c(21)	x(-18)	2121: y(3)	c(22)	x(-19)	c(23)	x(-20)
2112: y(2)	c(20)	x(-18)	c(21)	x(-19)	2122: y(2)	c(22)	x(-20)	c(23)	x(-21)
2113: y(1)	c(20)	x(-19)	c(21)	x(-20)	2123: y(1)	c(22)	x(-21)	c(23)	x(-22)
2114: y(0)	c(20)	x(-20)	c(21)	x(-21)	2124: y(0)	c(22)	x(-22)	c(23)	x(-23)

Fig. 22

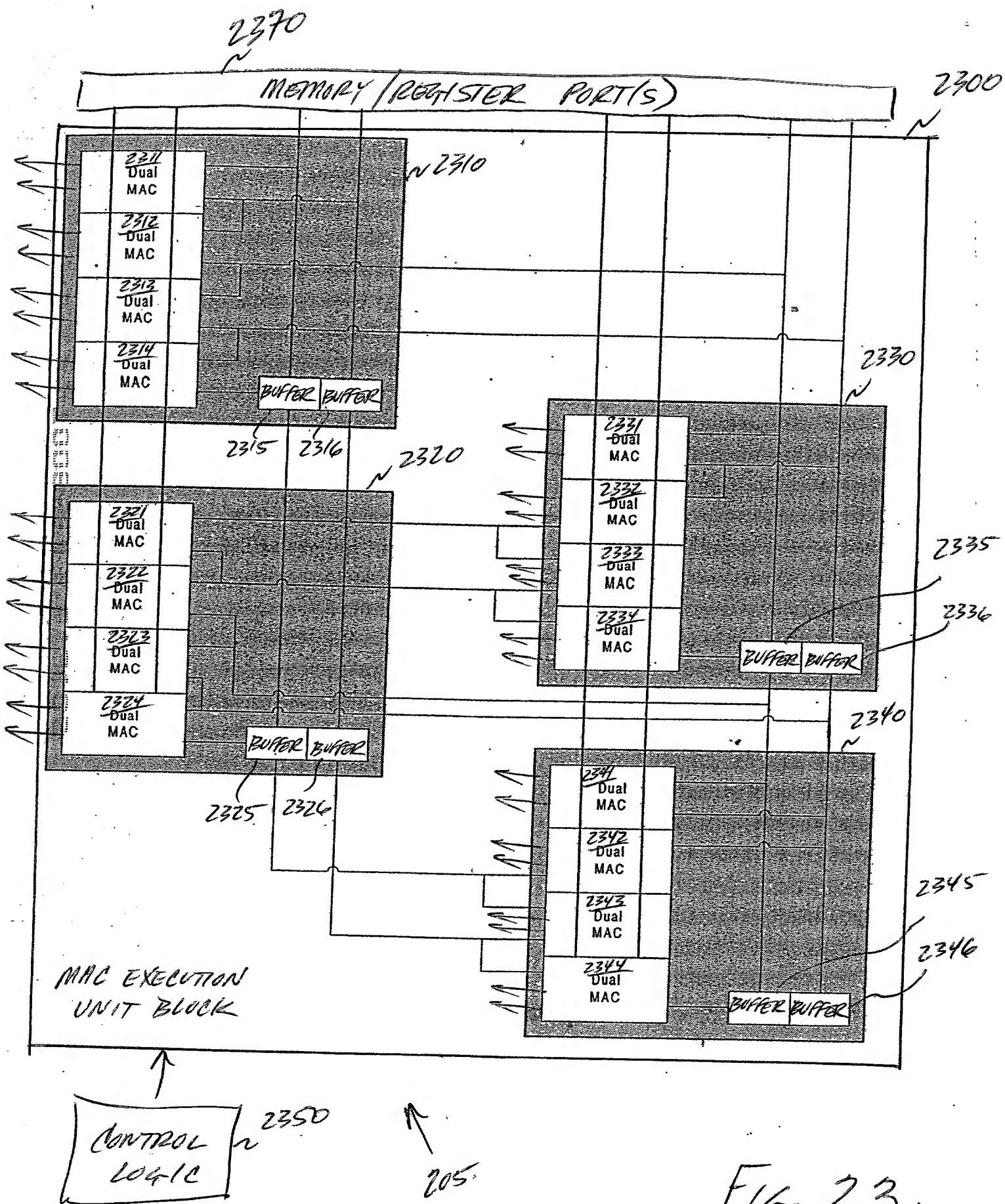
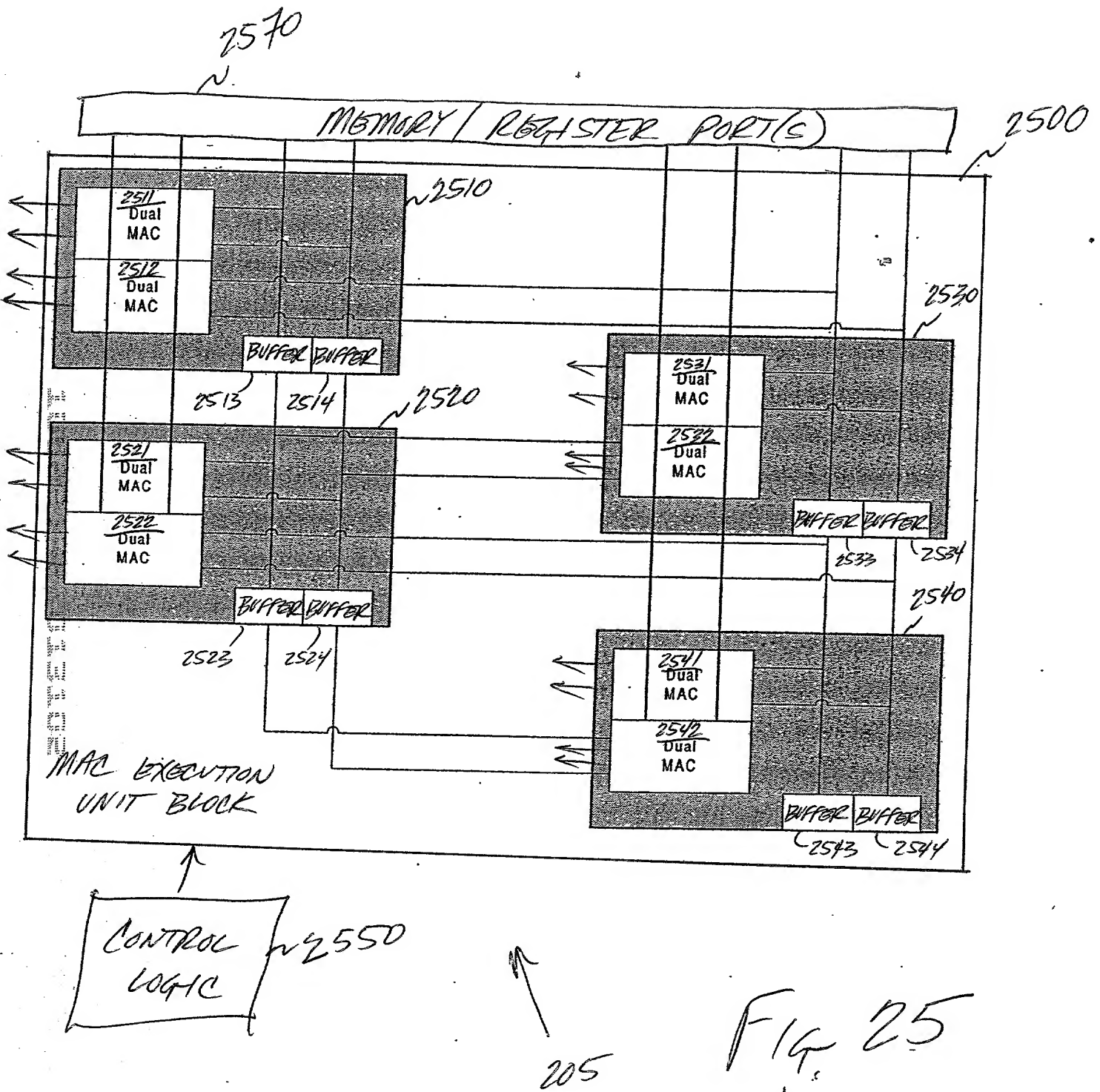


FIG. 23.

2400

Computation Cycle N									
MAC	1 st MAC Input	3 rd MAC Input	2 nd MAC Input	4 th MAC Input	MAC	1 st MAC Input	3 rd MAC Input	2 nd MAC Input	4 th MAC Input
2311: y(7)	c(28)	x(-21)	c(29)	x(-22)	2331: y(7)	c(30)	x(-23)	c(31)	x(-24)
2312: y(6)	c(28)	x(-22)	c(29)	x(-23)	2332: y(6)	c(30)	x(-24)	c(31)	x(-25)
2313: y(5)	c(28)	x(-23)	c(29)	x(-24)	2333: y(5)	c(30)	x(-25)	c(31)	x(-26)
2314: y(4)	c(28)	x(-24)	c(29)	x(-25)	2334: y(4)	c(30)	x(-26)	c(31)	x(-27)
2321: y(3)	c(28)	x(-25)	c(29)	x(-26)	2341: y(3)	c(30)	x(-27)	c(31)	x(-28)
2322: y(2)	c(28)	x(-26)	c(29)	x(-27)	2342: y(2)	c(30)	x(-28)	c(31)	x(-29)
2323: y(1)	c(28)	x(-27)	c(29)	x(-28)	2343: y(1)	c(30)	x(-29)	c(31)	x(-30)
2324: y(0)	c(28)	x(-28)	c(29)	x(-29)	2344: y(0)	c(30)	x(-30)	c(31)	x(-31)
Computation Cycle N+1									
MAC	1 st MAC Input	3 rd MAC Input	2 nd MAC Input	4 th MAC Input	MAC	1 st MAC Input	3 rd MAC Input	2 nd MAC Input	4 th MAC Input
2311: y(7)	c(24)	x(-17)	c(25)	x(-18)	2331: y(7)	c(26)	x(-19)	c(27)	x(-20)
2312: y(6)	c(24)	x(-18)	c(25)	x(-19)	2332: y(6)	c(26)	x(-20)	c(27)	x(-21)
2313: y(5)	c(24)	x(-19)	c(25)	x(-20)	2333: y(5)	c(26)	x(-21)	c(27)	x(-22)
2314: y(4)	c(24)	x(-20)	c(25)	x(-21)	2334: y(4)	c(26)	x(-22)	c(27)	x(-23)
2321: y(3)	c(24)	x(-21)	c(25)	x(-22)	2341: y(3)	c(26)	x(-23)	c(27)	x(-24)
2322: y(2)	c(24)	x(-22)	c(25)	x(-23)	2342: y(2)	c(26)	x(-24)	c(27)	x(-25)
2323: y(1)	c(24)	x(-23)	c(25)	x(-24)	2343: y(1)	c(26)	x(-25)	c(27)	x(-26)
2324: y(0)	c(24)	x(-24)	c(25)	x(-25)	2344: y(0)	c(26)	x(-26)	c(27)	x(-27)
Computation Cycle N+2									
MAC	1 st MAC Input	3 rd MAC Input	2 nd MAC Input	4 th MAC Input	MAC	1 st MAC Input	3 rd MAC Input	2 nd MAC Input	4 th MAC Input
2311: y(7)	c(20)	x(-13)	c(21)	x(-14)	2331: y(7)	c(22)	x(-15)	c(23)	x(-16)
2312: y(6)	c(20)	x(-14)	c(21)	x(-15)	2332: y(6)	c(22)	x(-16)	c(23)	x(-17)
2313: y(5)	c(20)	x(-15)	c(21)	x(-16)	2333: y(5)	c(22)	x(-17)	c(23)	x(-18)
2314: y(4)	c(20)	x(-16)	c(21)	x(-17)	2334: y(4)	c(22)	x(-18)	c(23)	x(-19)
2321: y(3)	c(20)	x(-17)	c(21)	x(-18)	2341: y(3)	c(22)	x(-19)	c(23)	x(-20)
2322: y(2)	c(20)	x(-18)	c(21)	x(-19)	2342: y(2)	c(22)	x(-20)	c(23)	x(-21)
2323: y(1)	c(20)	x(-19)	c(21)	x(-20)	2343: y(1)	c(22)	x(-21)	c(23)	x(-22)
2324: y(0)	c(20)	x(-20)	c(21)	x(-21)	2344: y(0)	c(22)	x(-22)	c(23)	x(-23)

FIG. 24



2600
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Computation Cycle N									
MAC	1 st MAC Input	3 rd MAC Input	2 nd MAC Input	4 th MAC Input	MAC	1 st MAC Input	3 rd MAC Input	2 nd MAC Input	4 th MAC Input
2511: y(6)	c(28)	x(-22)	c(29)	x(-23)	2531: y(6)	c(30)	x(-24)	c(31)	x(-25)
2512: y(4)	c(28)	x(-24)	c(29)	x(-25)	2532: y(4)	c(30)	x(-26)	c(31)	x(-27)
2521: y(2)	c(28)	x(-26)	c(29)	x(-27)	2541: y(2)	c(30)	x(-28)	c(31)	x(-29)
2522: y(0)	c(28)	x(-28)	c(29)	x(-29)	2542: y(0)	c(30)	x(-30)	c(31)	x(-31)
Computation Cycle N+1									
MAC	1 st MAC Input	3 rd MAC Input	2 nd MAC Input	4 th MAC Input	MAC	1 st MAC Input	3 rd MAC Input	2 nd MAC Input	4 th MAC Input
2511: y(6)	c(24)	x(-18)	c(25)	x(-19)	2531: y(6)	c(26)	x(-20)	c(27)	x(-21)
2512: y(4)	c(24)	x(-20)	c(25)	x(-21)	2532: y(4)	c(26)	x(-22)	c(27)	x(-23)
2521: y(2)	c(24)	x(-22)	c(25)	x(-23)	2541: y(2)	c(26)	x(-24)	c(27)	x(-25)
2522: y(0)	c(24)	x(-24)	c(25)	x(-25)	2542: y(0)	c(26)	x(-26)	c(27)	x(-27)
Computation Cycle N+2									
MAC	1 st MAC Input	3 rd MAC Input	2 nd MAC Input	4 th MAC Input	MAC	1 st MAC Input	3 rd MAC Input	2 nd MAC Input	4 th MAC Input
2511: y(6)	c(20)	x(-14)	c(21)	x(-15)	2531: y(6)	c(22)	x(-16)	c(23)	x(-17)
2512: y(4)	c(20)	x(-16)	c(21)	x(-17)	2532: y(4)	c(22)	x(-18)	c(23)	x(-19)
2521: y(2)	c(20)	x(-18)	c(21)	x(-19)	2541: y(2)	c(22)	x(-20)	c(23)	x(-21)
2522: y(0)	c(20)	x(-20)	c(21)	x(-21)	2542: y(0)	c(22)	x(-22)	c(23)	x(-23)

Fig. 26

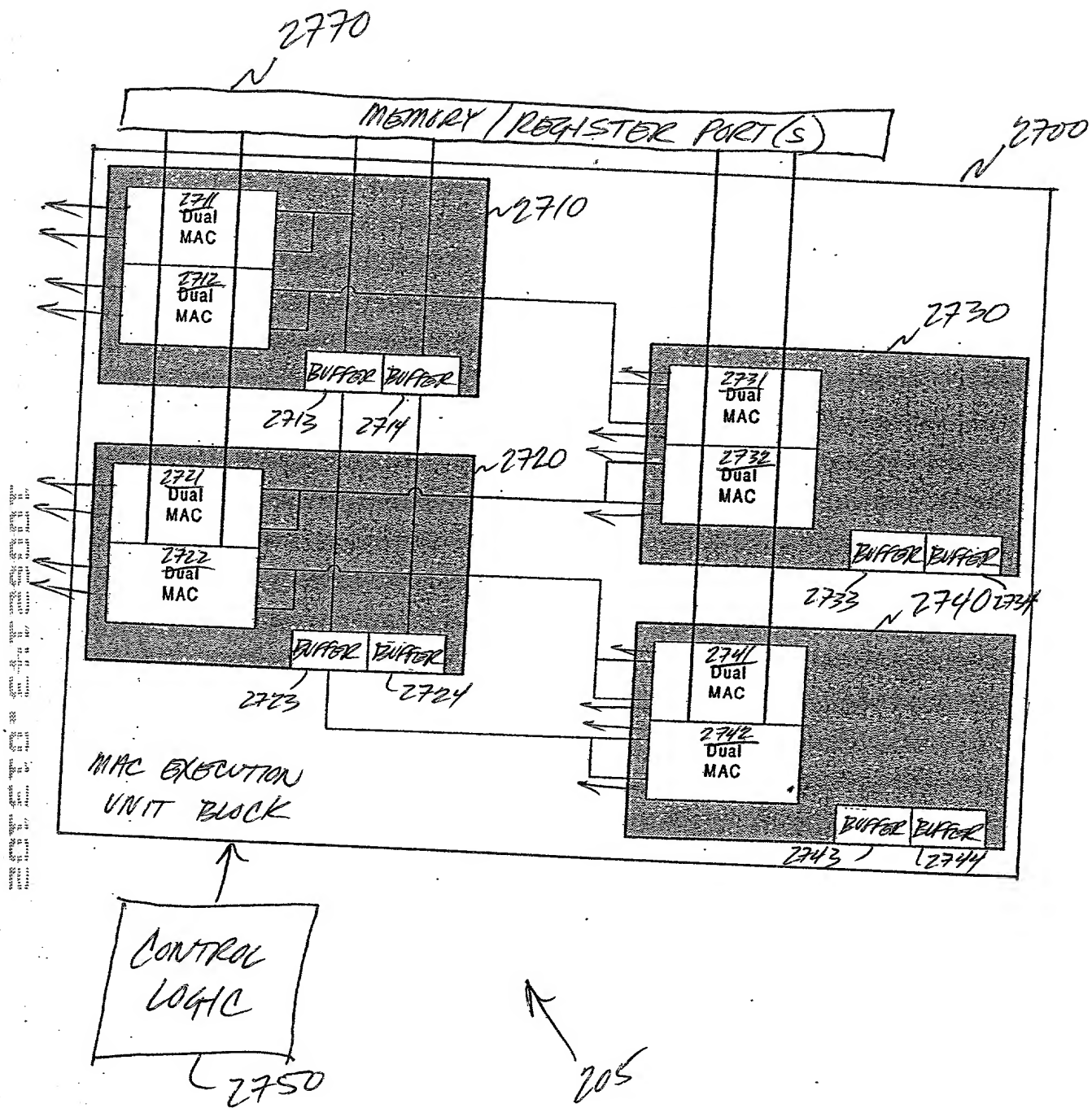


FIG. 27

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↓

Computation Cycle N											
MAC		1 st MAC Input	3 rd MAC Input	2 nd MAC Input	4 th MAC Input	MAC		1 st MAC Input	3 rd MAC Input	2 nd MAC Input	4 th MAC Input
2711	y(7)			c(29)	x(-19)	2731	y(7)			c(31)	x(-20)
	y(6)	c(28)	x(-19)				y(6)	c(30)	x(-20)		
2712	y(5)			c(29)	x(-20)	2732	y(5)			c(31)	x(-21)
	y(4)	c(28)	x(-20)				y(4)	c(30)	x(-21)		
2721	y(3)			c(29)	x(-21)	2741	y(3)			c(31)	x(-22)
	y(2)	c(28)	x(-21)				y(2)	c(30)	x(-22)		
2722	y(1)			c(29)	x(-22)	2742	y(1)			c(31)	x(-23)
	y(0)	c(28)	x(-22)				y(0)	c(30)	x(-23)		
Computation Cycle N+1											
MAC		1 st MAC Input	3 rd MAC Input	2 nd MAC Input	4 th MAC Input	MAC		1 st MAC Input	3 rd MAC Input	2 nd MAC Input	4 th MAC Input
2711	y(7)			c(25)	x(-17)	2731	y(7)			c(27)	x(-18)
	y(6)	c(24)	x(-17)				y(6)	c(26)	x(-18)		
2712	y(5)			c(25)	x(-18)	2732	y(5)			c(27)	x(-19)
	y(4)	c(24)	x(-18)				y(4)	c(26)	x(-19)		
2721	y(3)			c(25)	x(-19)	2741	y(3)			c(27)	x(-20)
	y(2)	c(24)	x(-19)				y(2)	c(26)	x(-20)		
2722	y(1)			c(25)	x(-20)	2742	y(1)			c(27)	x(-21)
	y(0)	c(24)	x(-20)				y(0)	c(26)	x(-21)		
Computation Cycle N+2											
MAC		1 st MAC Input	3 rd MAC Input	2 nd MAC Input	4 th MAC Input	MAC		1 st MAC Input	3 rd MAC Input	2 nd MAC Input	4 th MAC Input
2711	y(7)			c(21)	x(-15)	2731	y(7)			c(23)	x(-16)
	y(6)	c(20)	x(-15)				y(6)	c(22)	x(-16)		
2712	y(5)			c(21)	x(-16)	2732	y(5)			c(23)	x(-17)
	y(4)	c(20)	x(-16)				y(4)	c(22)	x(-17)		
2721	y(3)			c(21)	x(-17)	2741	y(3)			c(23)	x(-18)
	y(2)	c(20)	x(-17)				y(2)	c(22)	x(-18)		
2722	y(1)			c(21)	x(-18)	2742	y(1)			c(23)	x(-19)
	y(0)	c(20)	x(-18)				y(0)	c(22)	x(-19)		

Fig. 28